Amendments to the Claims

This listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims:

1. (Currently Amended). A circuit for accurately delivering a first stimulus voltage to one or more circuit nodes of an IC, said circuit comprising:

first switching means, within the IC, for conveying a force voltage to one of said circuit nodes via a first pin of said IC;

second switching means, within the IC, for conveying a sense voltage from said one of said circuit nodes via a second pin of said IC;

amplifier means for adjusting said force voltage to cause said sense voltage to equal said stimulus voltage;

storage means for storing a voltage difference between the force voltage and the sense voltage; and

means for selectively simultaneously enabling both of said switching means to enable said first stimulus voltage to be delivered to said one of said circuit nodes.

2. (Currently Amended). A circuit as defined in claim **1**, further including third switching means for selectively applying a second stimulus voltage to said circuit node whenever the first stimulus voltage is not being delivered to said circuit node.

3. (Currently Amended). A circuit as defined in claim **1**, each said switching means including transmission gates.

4. (Original). A circuit as defined in claim **1**, each said switching means being selectively controlled by a periodic signal.

5. (Original). A circuit as defined in claim **4**, said periodic signal for each of said switching means having different timing for rising and falling edges.

6. (Original). A circuit as defined in claim **1**, said storage means being a capacitor.

7. (Currently Amended). A circuit as defined in claim **1**, said integrated circuit having a scan register having a scan bit associated with said one of said circuit nodes, each said switching means enabled by the scan bit.

8. (Currently Amended). A circuit as defined in claim **1**, said integrated circuit having a scan register having a scan bit associated with said one of said circuit nodes, each said switching means enabled by the scan bit and a periodic signal.

9. (Original). A circuit as defined in ~~claim 1~~claim **2**, further including second amplifier means for sensing and forcing said second stimulus voltage, and said switching means for selectively applying a second stimulus voltage including separate switching means for force and sense signal paths similar to the switching means for said first stimulus voltage.

10. (Withdrawn). A method for accurately delivering a voltage to a circuit node of an integrated circuit, said integrated circuit having analog buses and transmission gates selectively connecting said circuit node to said buses, comprising:

sensing the voltage on the circuit node via a first of said buses under control of a first periodic signal;

applying a first stimulus voltage to said circuit node via a second bus under control of a second periodic signal;

applying a second stimulus voltage to said circuit node under control of a third periodic signal which is inverted with respect to said second periodic signal so that said circuit node is driven alternately to said first stimulus voltage and to said second stimulus voltage.

11. (Withdrawn). A method for accurately delivering, during testing, a first stimulus voltage to a circuit node of an integrated circuit having analog buses and transmission gates selectively connecting said circuit node to said buses, said method comprising:

establishing a voltage sense path from said circuit node to sense the voltage of said circuit node via one of said buses and a sense path transmission gate;

establishing a voltage force path to a circuit node which is to receive said first stimulus voltage via another of said buses and a force path transmission gate;

establishing a second stimulus voltage path to said circuit node;

applying a first periodic signal having a desired stimulus frequency to a control input of said force path transmission gate connected to said circuit node;

applying a second periodic signal to said sense path transmission gate, said second periodic signal having the same frequency as said first periodic signal; and

applying a third periodic signal having the same frequency as said first periodic signal, and which has an active time which is non-overlapping with an active time of the waveform of said first and second periodic signals so that the circuit node is not driven simultaneously by said first stimulus voltage and said second stimulus voltage.

12. (Withdrawn). A method as defined in claim **11**, wherein said second stimulus voltage path comprises a voltage sense path and a voltage force path, similar to the first stimulus voltage paths, and said third periodic signal controls the voltage force path for said second stimulus voltage, further including applying a fourth periodic signal to the voltage sense path for said second stimulus voltage and having the same frequency as said third periodic signal.

13. (New). A circuit for accurately delivering a stimulus voltage to one or more circuit nodes of an IC, said circuit comprising:

first switching means, within the IC, for conveying a force voltage to one of said circuit nodes;

second switching means, within the IC, for conveying a sense voltage from said one of said circuit nodes;

each said switching means being selectively controlled by a periodic signal;

amplifier means for adjusting said force voltage to cause said sense voltage to equal said stimulus voltage;

storage means for storing a voltage difference between the force voltage and the sense voltage; and

means for selectively simultaneously enabling both of said switching means to enable said first stimulus voltage to be delivered to said one of said circuit nodes.